CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

patterning a polysilicon layer formed over a silicon-containing region of a substrate so as to obtain a polysilicon feature;

forming a first metal silicide adjacent to said polysilicon feature while covering a top surface and sidewalls of said polysilicon feature;

doping said polysilicon feature after forming said first metal silicide;

exposing said top surface; and

forming a second metal silicide in said polysilicon feature, said second metal silicide differing from said first metal silicide.

2. The method of claim 1, wherein patterning said polysilicon feature includes forming a cover layer on said polysilicon layer and forming said polysilicon feature by lithography and anisotropic etching, whereby a non-removed portion of said cover layer serves to cover said top surface during the formation of said first metal silicide.

3. The method of claim 2, further comprising adjusting optical characteristics of said cover layer so as to act as a bottom anti-reflective coating.

4. The method of claim 2, further comprising adjusting at least one of a composition and a thickness of said cover layer so as to hinder ion penetration into said polysilicon feature during a following ion implantation.

5. The method of claim 1, wherein said second metal silicide comprises nickel monosilicide.

6. The method of claim 5, wherein said first metal silicide comprises cobalt disilicide.

7. The method of claim 2, wherein said top surface is exposed by anisotropically etching said non-removed portion of said cover layer.

8. The method of claim 1, further comprising forming sidewall spacers to cover the sidewalls of said polysilicon feature.

9. The method of claim 5, further comprising forming doped areas adjacent to said polysilicon feature prior to forming said first metal silicide region.

10. The method of claim 9, wherein exposing said top surface includes an isotropic etch process.

11. The method of claim 9, further comprising doping said polysilicon feature prior to forming a nickel silicide region and after forming said first metal silicide.

12. The method of claim 11, further comprising forming an implantation mask above said first metal silicide.

13. The method of claim 12, further comprising forming an etch stop layer above said second metal silicide.

14. The method of claim 13, further comprising forming a dielectric layer above said polysilicon feature and said implantation mask, and forming contact holes to said first metal silicide and said second metal silicide.

15. The method of claim 5, wherein forming said nickel silicide region includes depositing a nickel layer, heating said substrate to initiate a chemical reaction between silicon and nickel, and selectively removing non-reacted nickel.

16. A method of forming a field effect transistor, the method comprising:

forming a layer stack including at least a gate insulation layer, a polysilicon layer and a cap layer above a silicon region formed on a substrate;

patterning said layer stack to form a gate electrode having a top surface covered by at least said cap layer;

forming a drain and a source region adjacent to said gate electrode;

forming silicide regions comprising a first metal in said drain and source regions;

doping said gate electrode after forming said first metal silicide;

exposing said top surface of said gate electrode; and

forming a silicide region comprising a second metal in said gate electrode.

17. The method of claim 16, wherein said cap layer is formed so as to act as a bottom anti-reflective coating during patterning said layer stack.

18. The method of claim 16, further comprising forming sidewall spacers at sidewalls of said gate electrode.

19. The method of claim 18, wherein exposing said top surface includes performing an anisotropic etch process to remove material of said cap layer.

20. The method of claim 19, wherein exposing said top surface includes an isotropic etch process.

21. The method of claim 16, further comprising implanting a dopant species into said gate electrode prior to forming said second metal silicide region and after forming said first metal silicide region.

22. The method of claim 16, further comprising implanting a dopant species into said gate electrode prior to forming said first and second metal silicide regions.

23. The method of claim 16, wherein said first metal silicide region is comprised of cobalt disilicide.

24. The method of claim 23, wherein said second metal silicide region is comprised of nickel silicide.

25. A field effect transistor, comprising:

a gate electrode formed on a gate insulation layer;

a nickel silicide region formed on said gate electrode;

a drain region and a source region formed adjacent to said gate electrode; and

a metal silicide region formed in said drain and source regions, wherein said metal silicide region is comprised of a metal silicide other than nickel silicide.

26. The field effect transistor of claim 25, wherein said metal silicide region is comprised of cobalt disilicide.